34. (New) An instruction conversion apparatus that converts an instruction sequence into object codes including a plurality of parallel execution codes capable of being executed by a processor in parallel, comprising:

an instruction scheduling unit that schedules instructions in the instruction sequence for the parallel execution codes, a bit length of the instructions and the parallel execution codes being variable,

wherein each of the parallel execution codes include up to N pieces of the instructions, and a total bit length of each of the parallel execution codes is shorter than the sum of bit length of N pieces of the longest bit length of the instructions.

35. (New) The instruction conversion apparatus of claim 34,

wherein the parallel execution codes have a special bit which instructs the target processor to execute a plurality of instructions of the parallel execution codes in parallel.

36. (New) The instruction conversion apparatus of claim 35,

wherein the instruction scheduling unit controls the special bit so that a total word length of an individual parallel execution code is shorter than a bit length of N pieces of the longest bit length of the instructions.

37. (New) The instruction conversion apparatus of claim 34,

wherein the instruction sequence is written in a high-level language before converting into object codes.

38. (New) A processor that executes the instruction sequence converted into the object codes by the instruction conversion apparatus of claim 34.

39. (New) The processor of claim 38, further comprising:

an instruction supplying/issuing unit for fetching an instruction sequence and outputting the instruction sequence;

a decoding unit for decoding the parallel execution codes successively; and

an execution unit for executing a plurality of instructions in parallel in accordance with a decoding result of the decoding unit.

40 (New) A processor comprising:

an execution unit capable of executing up to N number of instructions having a variable bit length in parallel, N being an integer which is at least two;

an instruction supplying/issuing unit which fetches an instruction sequence in a unit of a first bit length of code and outputs the instruction sequence in a unit of a second bit length of code, the second bit length being shorter than a bit length of N number of instructions having the longest bit length; and

a decoding unit which decodes the instruction sequence in a unit of a variable bit length of code which is at least a part of the second bit length of code outputted by the instruction supplying/issuing unit, and outputting a decoding result to the execution unit.

41. (New) The processor of claim 40,

wherein the instruction sequence is converted by a certain instruction conversion apparatus.

42. (New) The processor of claim 41,

wherein the instruction sequence is written in a high-level language before being converted by the instruction conversion apparatus.

43. (New) The processor of claim 40,

wherein the first bit length is shorter than the second bit length.

44. (New) The processor of claim 40,

wherein at least a part of the instructions have a special bit which instructs the target processor to execute a plurality of instructions in parallel.

45. (New) The processor of claim 40,

wherein the decoding unit comprises:

an instruction issuing control unit which identifies instruction boundaries executed in parallel.

46. (New) The processor of claim 40,

wherein instruction supplying/issuing unit comprising:

a fetch unit for successively fetching the instruction sequence; and

a plurality of instruction buffers for temporally storing instructions.

47. (New) A processor comprising:

an instruction fetching unit that fetches instructions, each instruction having a variable bit length;

a decoding unit that decodes the instructions;

an execution unit that executes up to N number of decoded instructions from the decoding unit, N being an integer which is at least two,

wherein the decoded instructions are a variable bit length which are not related to the bit length of the fetched instructions, and the total bit length of the decoded instructions is shorter than the sum of the bit length of N number of the longest bit length of the instructions.

48. (New) The processor of claim 47,

wherein the instruction sequence is converted by a certain instruction conversion apparatus.

49. (New) The processor of claim 48,

wherein the instruction sequence is written in a high-level language before being converted by the instruction conversion apparatus.

50. (New) The processor of claim 47,

wherein the instruction fetching unit fetches an instruction sequence in a unit of a first bit length of code and outputs the instruction sequence in a unit of a second bit length of code, the first bit length being shorter than the second bit length.

51. (New) The processor of claim 47,

wherein at least a part of the instructions have a special bit which instructs the target processor to execute a plurality of instruction in parallel.

52. (New) The processor of claim 47,

wherein the decoding unit comprises:

an instruction issuing control unit which identifies instruction boundaries executed in parallel.

53. (New) The processor of claim 47, further comprising:

a plurality of operation execution units capable of executing a plurality of instructions in parallel in accordance with a decoding result of the decoding unit.

54. (New) The processor of claim 47,

wherein instruction fetching unit comprising:

a fetch unit for successively fetching the instruction sequence; and

a plurality of instruction buffers for temporally storing instructions.